

**Amendments to the Claims**

This listing of claims will replace all prior versions, and listings, of claims in the application:

**Listing of Claims:**

1. - 3. (Cancelled).

4. (Previously presented) A sampling circuit for an analog signal according to a clock signal, comprising:

a first thin film transistor (TFT), having a first electrode to receive the analog signal, a control electrode to receive the clock signal and a second electrode for sampling the analog signal when the clock signal is at a first logic level; and

a counteracting device coupled to the second electrode and comprising:

an inversion device, having an input terminal coupled to the control electrode; and

a second TFT having a gate terminal coupled to an output terminal of the inversion device and a source and drain terminal both coupled to the second electrode;

wherein when the clock signal is changed from the first logic level to a second logic level, the counteracting device reduces a feed-through voltage drop caused by a parasitic capacitor between the second electrode and the control electrode of the first TFT.

5. - 7. (Cancelled)

8. (Previously presented) A liquid crystal display, comprising:

a plurality of display units, arranged in an array;

a plurality of data lines disposed corresponding to each line of the display units, wherein each data line provides a video signal to the corresponding display unit; and

a data driving circuit, having at least one sampling circuit, sampling an image signal to be the video signal according to a clock signal, and the sampling circuit comprising:

a first thin film transistor (TFT), having a first electrode receiving an analog signal, a control electrode receiving the clock signal, and a second electrode for sampling the analog signal when the clock signal is at a first logic level; and

a counteracting device coupled to the second electrode and comprising:

an inversion device, having an input terminal coupled to the control electrode; and

a second TFT having a gate terminal coupled to an output terminal of the inversion device and a source and drain terminal, both coupled to the second electrode;

wherein when the clock signal is changed from the first logic level to a second logic level, the counteracting device reduces a feed-through voltage drop caused by a parasitic capacitor between the second electrode and the control electrode of the first TFT.

9. (Previously presented) A sampling circuit for an analog signal according to a clock signal, comprising:

a first thin film transistor (TFT), having a first electrode to receive the analog signal, a control electrode to receive the clock signal and a second electrode for sampling the analog signal when the clock signal is at a first logic level; and

a counteracting device coupled to the second electrode and comprising:

an inversion device, having an input terminal coupled to the control electrode; and

a capacitor between the second electrode and an output terminal of the inversion device;

wherein when the clock signal is changed from the first logic level to a second logic level, the counteracting device reduces a feed-through voltage drop caused by a parasitic capacitor between the second electrode and the control electrode of the first TFT.

10. (Currently amended) The circuit as claimed in claim 9, wherein the first TFT is an ~~NMOA~~ NMOS transistor.

11. (Previously presented) A liquid crystal display, comprising:

a plurality of display units, arranged in an array;

a plurality of data lines disposed corresponding to each line of the display units, wherein each data line provides a video signal to the corresponding display unit; and

a data driving circuit, having at least one sampling circuit, sampling an image signal to be the video signal according to a clock signal, and the sampling circuit

comprising:

a first thin film transistor (TFT), having a first electrode to receive the analog signal, a control electrode to receive the clock signal and a second electrode for sampling the analog signal when the clock signal is at a first logic level; and

a counteracting device coupled to the second electrode and comprising:

an inversion device, having an input terminal coupled to the control electrode; and

a capacitor between the second electrode and an output terminal of the inversion device;

wherein when the clock signal is changed from the first logic level to a second logic level, the counteracting device reduces a feed-through voltage drop caused by a parasitic capacitor between the second electrode and the control electrode of the first TFT.

12. (Currently amended) The circuit as claimed in claim 11, wherein the first TFT is an ~~NMOS~~ NMOS transistor.